

Active Noise Regulation

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Introduction

The increasing importance of effective power integrity management for Nanoprocessors and ULSI chips has been well documented. Yield loss and timing problems undetected by traditional verification methods may be traced to a decrease in supply noise margin in components using advanced fabrication processes at and below the 90nm node. A combination of increased current density at lower supply voltages and supply pathway impedance results in large, on and off chip, relative supply variations called voltage droops in the literature [1]. These fluctuations make it more difficult to reduce static and dynamic power consumption by further reductions in supply voltage. Simultaneously, finer dimension nanometer processes (90nm and below) exhibit very substantial device variances during manufacturing, necessitating more stringent supply voltage control and lesser supply voltage variation.

Traditional techniques to minimize supply noise such as voltage positioning and on-chip decoupling capacitor integration are difficult to apply in addressing high-bandwidth power integrity needs. Due to the exponential rise of gate leakage in sub 100nm processes, on-chip decoupling is an unacceptable choice for dynamic noise mitigation. Energy stored in integrated capacitors diminishes quadratically with supply voltage. It has also been shown in the art that the scaling of package filter component characteristics, such as the loop inductance of on-package capacitors, and the series resistance of the power path, will be impractically exponential [1, Power Delivery section]. In this paper, we introduce the techniques of active noise regulation (ANR) and active VLSI packaging (AVP), methods that take advantage of proximity to the load component to place stable, large charge reservoirs where they are most needed.

ANR

Active Noise Regulation addresses noise through rapid, controlled and local supply of charge into the load component power grid. Figure 1 illustrates the implementation of an ANR component shown simply as a FET switch device. The ANR is associated with a dedicated 'Reservoir' capacitor that is either fed by a supply line connecting to an external, high-voltage power supply or is charge-pumped as determined by the system design. This provides the ANR with a reservoir of charge that is many times greater than charge stored at the load component's operating voltage. The ANR (or an array of ANR's) connects to the load component by very short lengths of interconnect as in figure 4. The ANR is therefore fully cognizant of the spatial and temporal variation of the load component power supply voltages. In a 'droop' event, it initiates compensating flow of charge from the Reservoir Cap into the load power grid. After a brief duration of high current and charge flow, the ANR shuts the current flow in a controlled manner.

Figure 2 is a 3-D view of time-varying noise on a ULSI chip power grid output by an EDA tool PowerESL. The left hand side of the plot shows 40% lower noise in the grid response to an identical load current with ANR functionality included. While droops have been specifically addressed, ANR's can just as effectively address overshoots.

Leakage & voltage dependence of noise

Figure 5 shows a simplified model of the system power grid. It can be seen from the equations that a large static leakage component can provide an overall reduction in on-chip noise. However, large static leakage contributes significantly to the overall power consumption as well as to local peak currents thus rendering much larger total noise.

In power networks with high Q, the grid continues to oscillate for some cycles after the noise source has been switched off. In other words, low dissipation systems also have much greater dynamic voltage droops, particularly at frequencies around resonant frequency points. ANR's provide designers with the means to reduce noise in low-loss delivery systems. Using ANR the system Q is increased, not by reducing resistance, but by taking advantage of the quadratic increase in capacitive energy with voltage to place large amounts of energy at or near the load. The advantages of low loss power transport at high voltage followed by voltage conversion at the load have been well known since the early days of power distribution. ANR's provide this benefit in high-speed systems.

AVP

A severe limitation in the capability of integrated or on-chip capacitors in storing charge follows from (10) and the fact that MOSFET devices push reliability limits. A key limitation of passive devices such as package capacitors is that they are 'reactive' devices. In Active VLSI Packaging (AVP), package capacitors are combined with land-side mounted ANR devices (Figure 4). This technique thus allows active control of dynamic noise with minimal additional power. Also, active noise regulators provide a means for introducing dynamic damping impedances into the power delivery system, pro-actively controlling supply resonances.

Conclusion

We have shown that active noise regulation can be used to effectively control noise in low loss power grids. A tool, PowerESL, has also been developed to accurately inspect on-chip dynamic power noise so as to design in the benefits of ANR's and AVP.

[1] R. Mahajan, Raj Nair et al., "Emerging Directions for Packaging Tech.", Intel Technology Journal 2002

[2] Jan. 2006 Power Management Designline article <http://www.powermanagementdesignline.com/howto/175800373>

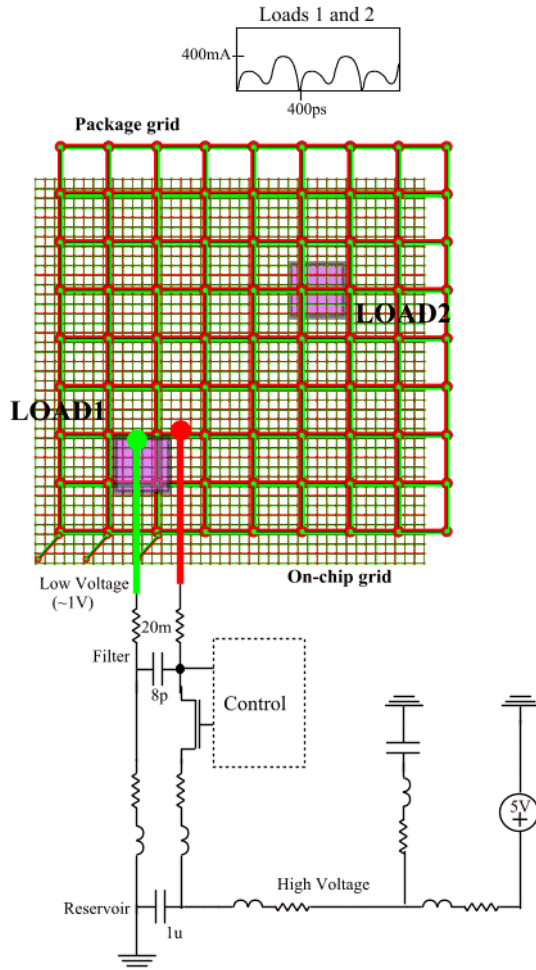


Figure 1: ANR connectivity

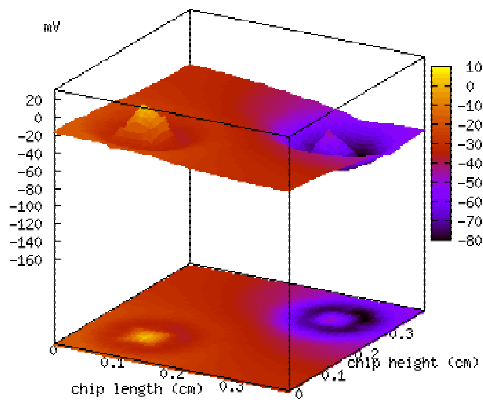


Figure 2: Lower noise by ANR Charge Boosting

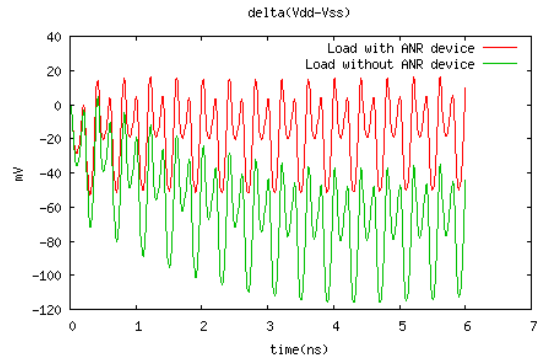


Figure 3: Noise with & w/o ANR's

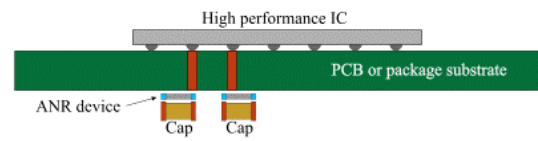


Figure 4: ANR implementation

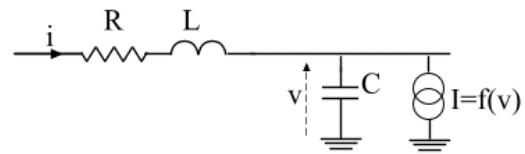


Figure 5: Simplified power integrity model

$$-v = iR + L \frac{di}{dt} \quad (1) \quad i = I + C \frac{dV}{dt} \quad (2)$$

$$-v = LC \frac{d^2v}{dt^2} + RC \frac{dv}{dt} + RI + L \frac{dI}{dt} \quad (3)$$

$$I = I_0 + gv \quad (4) \quad -v = (I_0 + gv)R \quad (5)$$

$$-v = \frac{I_0 R}{1 + gR} \quad (6)$$

$$v = v_0 \exp\left(-\frac{\omega_0 t}{2Q}\right) \cos\left(\omega_0 \sqrt{1 - \frac{1}{4Q^2}} t\right) \quad (7)$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (8) \quad Q = \frac{L\omega_0}{R} \quad (9)$$

$$Q_A = C_A V = \epsilon_r \epsilon_0 E \quad (10)$$