Enhancing Signal Integrity in Cables: DVI to HDMI and Class-B Differential Signaling

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Introduction

Prior papers "Cat 5 Cable Modeling for DVI/HDMI Links" [2] and "Bit Error Rate and Signal Integrity for Cat-5 based DVI / HDMI links" [3] discussed modeling Cat-5 UTP cables and verification of the feasibility of binary or digital signaling for DVI / HDMI over long (25m) Cat-5e links. This paper discusses aspects impacting signal integrity of binary signals transmitted over Cat-5e cables as well as techniques to enhance the quality of signals transmitted. We look at DVI and HDMI specifications, and particularly, electrical specifications within, and identify aspects in the HDMI specification that improve upon DVI as it relates to high-speed signal transmission over long cables. We also introduce symmetric true-differential signaling, called Class-B Differential Signaling (CBDS), conceived, developed and implemented in 180nm CMOS by ComLSI®, advancing the state of the art in differential signal transmission.

Of the various cable architectures in existence, the most common are co-axial cables and twisted wire pair assemblies. We will look primarily at twisted wire pair assemblies, given that they are extensively employed in electronics communications, have standards the industry follows, and are increasingly finding use in high-definition video/audio data distribution as well. Such cable assemblies used in nearly all computer-networking infrastructures have been categorized as Cat-5, Cat-5e, and Cat-6 etc. by the Telecommunications Industry Association (TIA) and the Electronics Industry Association (EIA). Cat-5e consists of 4 twisted wire pairs as shown in figure 1(a) held together by an outer jacket, which may include a conductive braid as a shield. Figure 1 also shows a cable assembly rated for 10Gbps data through put (10GBASE-T) from Systimax® [8]. Cat-5e has a rated bandwidth of 350MHz for each twisted wire paid within [6]. We will limit our discussion on cables and signal integrity (SI) to Cat-5e and other similar interconnect.

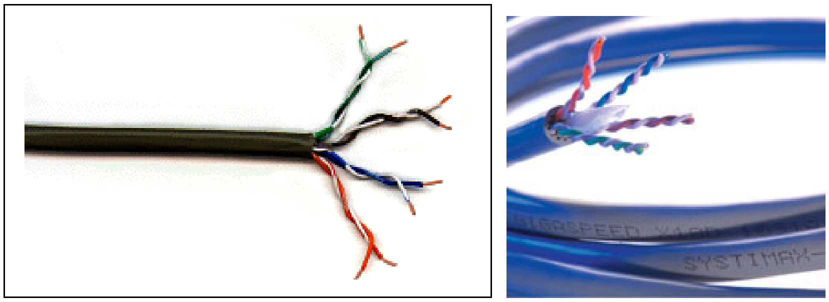

Figure 1: a) typical Cat-5e cable twisted wire pairs, b) Gigaspeed® cable from Systimax®

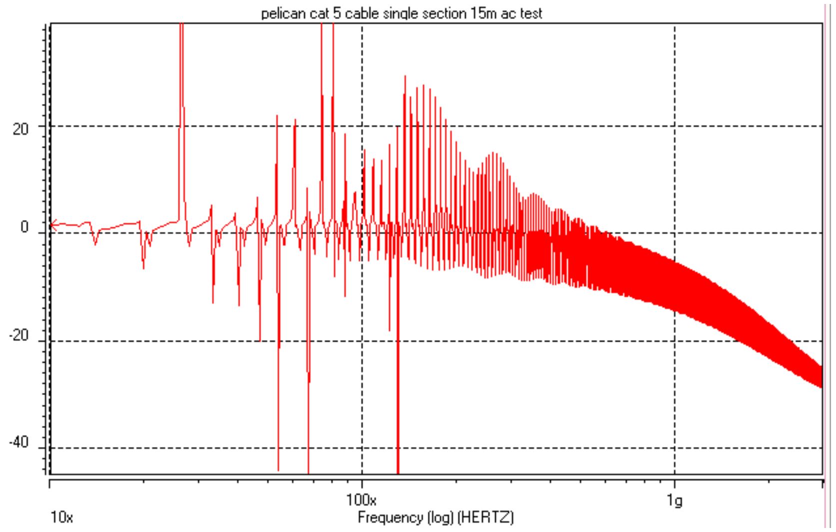

Figure 2: Cat-5 worst-case model [2], insertion dB loss vs. frequency, 15 meter length

Cable channel capacity and SNR

Shannon's theorem for channel capacity [7] combined with the 350MHz bandwidth rating of Cat-5e cables indicate that a signal-to-noise ratio (SNR) of about 30dB will permit robust transmission of up to 3.5Gbps per twisted wire pair. A key limitation to long cables such as those employed in DVI and HDMI applications is the attenuation of signals that leads to a low far-end SNR. While Cat-5e standards provide that attenuation in the cable is low (22dB for a 100 meter length) at a test frequency of 100Mhz, as the spectral content of the signal increases, losses along the cable length are quite high, as can be seen from the result of a worst-case model of a Cat-5 cable [2] shown in fig. 2.

The model [2] that emulates the behavior of an untwisted 15 meter Cat-5 cable shows that attenuation of signals at a frequency of 1.7GHz (corresponding to the fundamental frequency at a data rate of 3.4Gbps) can be as much as 1.2dB/meter.

Over a 25 meter length of cable, the spectral component corresponding to the fundamental of the data rate may see as much as a 30dB reduction in amplitude. Since receiver comparators need a minimum voltage signal to distinguish symbols, and since a certain SNR value is necessary to accomplish high data throughput, **signal gain** is essential within such long links. The interesting question is as to where this gain is best incorporated, which we'll get to in a further section.

Spectral Signal Balancing or Equalization

Figure 3 illustrates one of the many techniques employed to compensate for the non-linear attenuation of signal spectral content. Since high frequencies are attenuated substantially more than lower frequencies, gain is introduced into the high-frequency components of the transmitted signals.

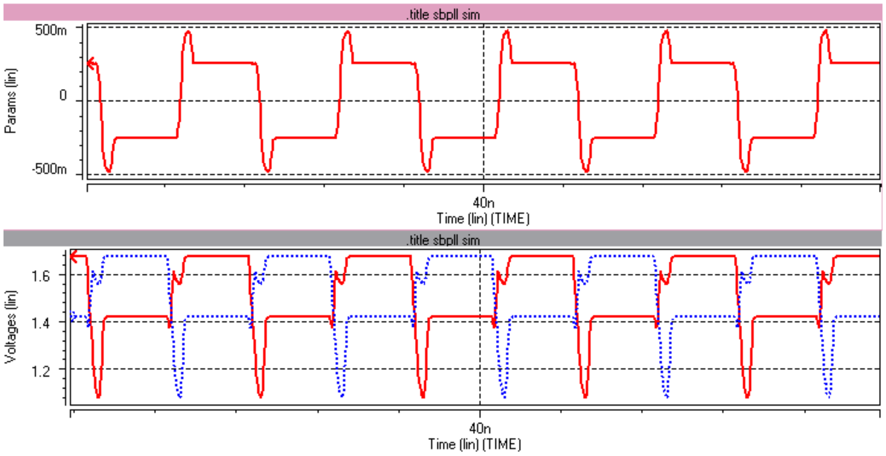

Figure 3: Post-cursor transmitter equalization (pre-emphasis)

This may be done pre-cursor, or post-cursor, or both, referring to the temporal or phase relationship between the added high-frequency signals to the transmitted signal. Pre-emphasis is typically practical when the transmitted signals are of a lower frequency, shown in figure 3. Here, the edge-frequency content of a differential signal transmitted (the two voltage signals are shown in the lower plot and the difference in the upper plot) is amplified to approximately twice the amplitude of the normal signal difference.

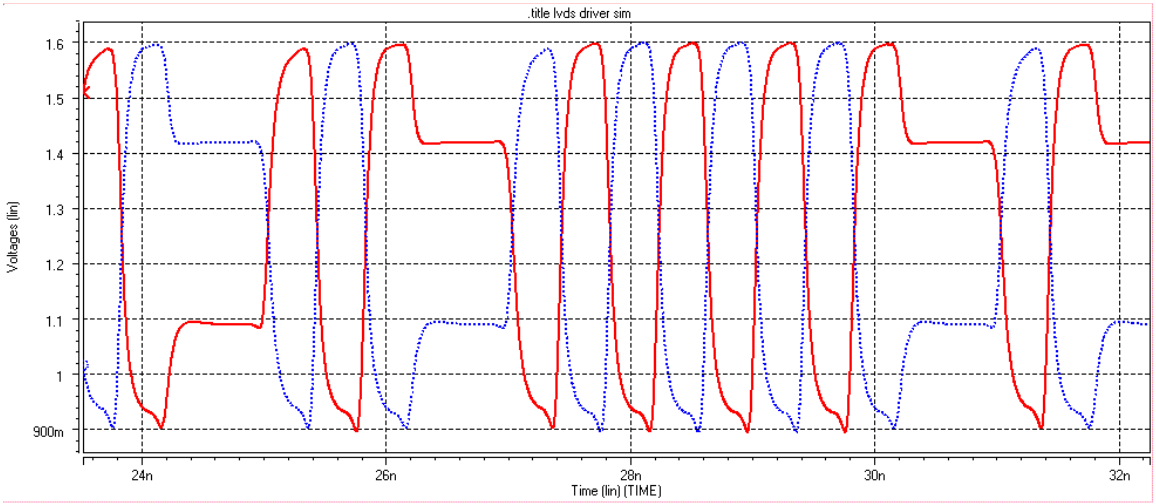

Figure 4: De-emphasis transmit equalization implementation

For high-frequency signals transmitted, de-emphasis is usually a more accurate and the preferred method, achieving essentially the same effect as pre-emphasis, albeit with lesser overall signal amplitude when the total swing is restricted. Here, based upon the previous symbol transmitted, the voltage transition developed is reduced for symbol sequences of the same type. The results of an implementation that approximately halves the transmitted signal for repeating symbols is shown in figure 4. De-emphasis is a more ‘digital’ technique, easier to implement, and the most commonly chosen technique for high-speed binary data transmission over lossy (long cable, for example) links. Multiple signal levels may be employed based upon channel and data run-length. Interestingly, **DVI** [10] does not specify any equalization at the transmitter or the receiver. A transition from Analog RGB signals requiring far lower cable bandwidth to digital, binary signaling greatly exceeding the cable bandwidth without signal pre-conditioning does not seem to make good sense. Constraints in the DVI specification for the Electrical Layer indicate limits to voltage overshoot (15%) and undershoot (25%) that limit transmit emphasis. **HDMI** [12] on the other hand, while continuing the legacy specifications of DVI, has relaxed this specification indicating that “*It is recommended that Sources capable of higher speeds incorporate an effective amount of source termination, especially if using Type C connectors. This termination will typically have the effect of lowering the average DC level of each single-ended signal. The relaxed VH and VL parameters permit such an implementation*”. Presumably, this relaxation may permit some form of transmit signal conditioning, though the absence of any description of this aspect is puzzling.

In addition to signal pre-conditioning that may be performed at the transmitter (source) end, signal balancing may also be carried out before, and at the receiver. Again, **DVI** makes no mention of any equalization that may be performed at the receiver (sink) end of the cable. **HDMI** deals with spectral balancing at the receiver through the following recommendation “*higher-speed HDMI Sinks are expected to support some sort of cable equalization function which allows them to recover data from such cables*“, which closely resembles passive equalization filters of the resonant variety [3] that assist in amplifying particular spectral components of the received signal. Additionally, there is reiteration in the **HDMI** specification [12] that “*The HDMI Sink is required to successfully recover the data stream from any compliant Sink input signal. At high frequencies, a compliant Sink input signal is any signal that, after application of the Reference Cable Equalizer to each of the differential TMDS signals, results in a signal that meets the Sink input eye requirements.*” This appears to leave well-known techniques in the art that implement active, finite impulse response (FIR) filter functions, or digital signal processing (DSP) techniques that open the data EYE for successful data recovery, to the discretion of the system designer.

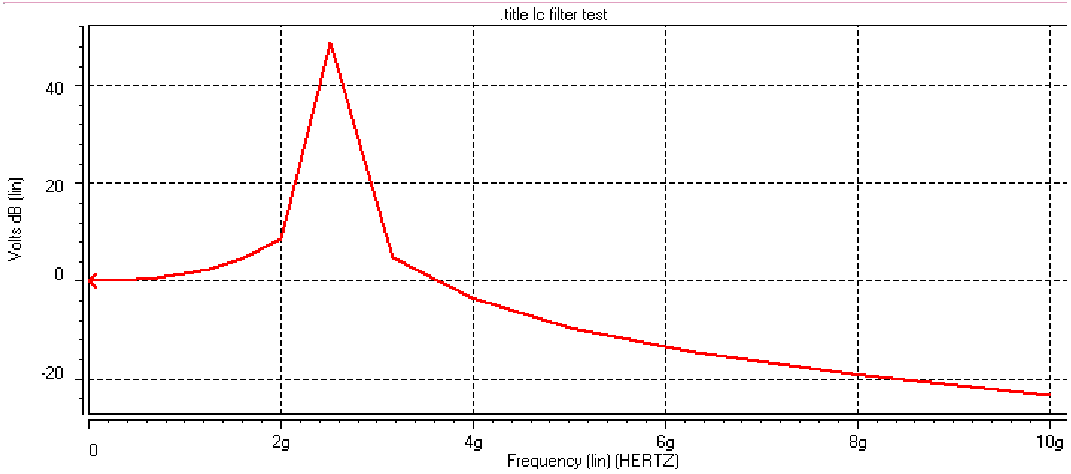

Figure 5: Simple LC resonant filter transfer function

Figure 5 indicates the transfer function response of an 'ideal' L-C resonant filter. Practical resonant filters will demonstrate far lower peak gain. Investigations conducted at ComLSI in 2005 [3] have shown that similar resonant filters applied to 2.5Gbps signals at the sink end of a 25 meter Cat-5 cable successfully open the received, closed data EYE with sufficient amplitude and width for robust data recovery. **HDMI 1.3a** [12] recommends such a '*Reference cable equalizer*' for compensation for high-frequency signal loss. The transfer function of this reference cable equalizer as shown in the specification indicates a gain of approximately 3 peaking at a frequency of roughly 2.5GHz, much alike the resonant filter investigated in ComLSI's 2.5Gbps per twisted-wire-pair link implemented in 0.18um CMOS.

What is truly interesting about such resonant filters is that with creative interconnect design (patent-pending technology at ComLSI), they may be constructed into the interconnect assembly itself, thereby rendering the interconnect 'active', or amplifying and to an extent, self-correcting. Such Active Interconnect can therefore compensate, in limited fashion, the loss of specific high-frequency components essential to high SNR in binary signaling.

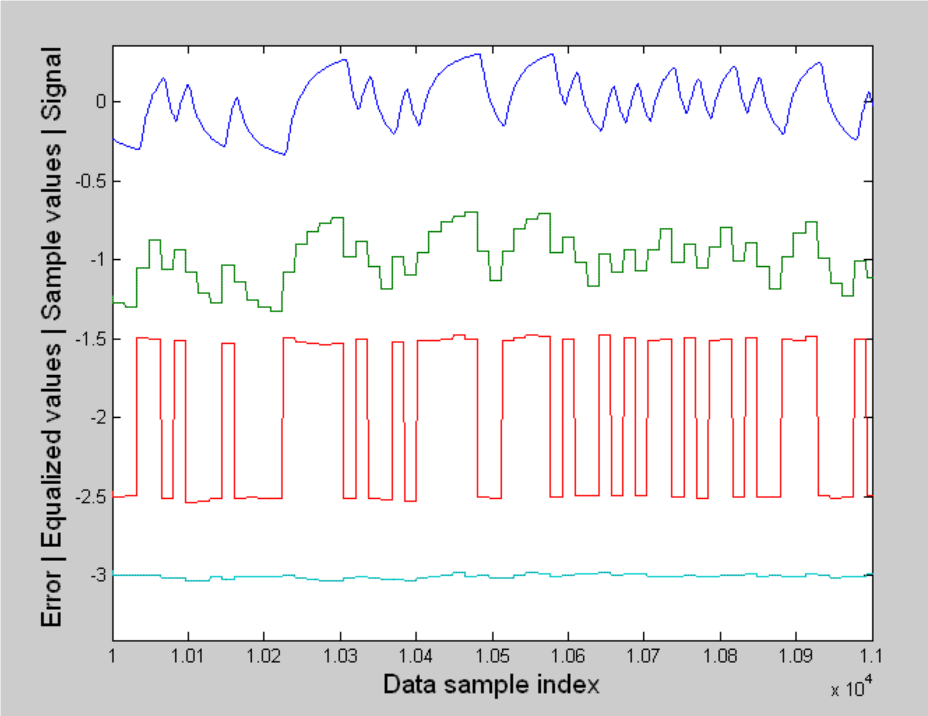

Figure 6: Channel-distorted signal, and FIR-based equalization [11]

Receiver Digital Signal Processing

A well known aspect of digital signal transmission over bandwidth limited channels is inter-symbol interference (ISI), which in simple terms may be thought of as the spreading that a digital pulse encounters as it passes along a lossy channel that attenuates signal spectral components in a non-linear manner. In other words, the energy of a single transmitted bit leaks into adjacent bits that follow it in time along the interconnect channel. While ISI is a consequence of the transfer function (or analog signal transmission characteristic) of the interconnect channel, it may be effectively corrected for using digital signal processing techniques such as finite impulse response (FIR) filters employed at either end of the transmission link. An illustration of the transformation of a bit stream and the eventual recovery of the stream is illustrated in Figure 6.

Figure 6 demonstrates the effectivity of a 3-bit FIR filter in correcting a received symbol sequence signal transformed by a bandwidth limited transfer function emulating an interconnect channel. Clearly, the integrity of the transmitted signal, diminished substantially by the channel transfer function is recovered entirely by the FIR filter. In a practical design, limitations (non-idealities) of the FIR implementation often require adaptation to ensure optimal counteraction of variable data rates and channel characteristics.

Whereas **DVI** fails to make any mention of receiver or sink equalization, **HDMI** explicitly cites it as a requirement for robust and low bit error rate data recovery. At the same time, HDMI dwells upon what it calls 'reference cable equalization' that discusses resonant spectral balancing in some depth, and reiterates the necessity of sink equalization at the receiver to meet the receiver EYE requirement. When using long cables, therefore, it will quickly be apparent to a link designer that a simple resonant filter compensator will need to be augmented by active equalization techniques such as the FIR filter equalizer to enhance SI. ComLSI's 25m 2.5Gbps per channel data link PHY employs digital signal processing in the form of 4-bit FIR filters integrated into the receivers to compensate for ISI and recover the data EYE for low bit error rate (BER) performance.

Source and Sink Termination

A fundamental aspect of signaling on transmission lines is line termination, both at the source and the sink ends of a link. Termination serves multiple purposes, which include the prevention of reflections from impedance discontinuities and provision of a load device across which a signal is developed. A less appreciated aspect of termination devices is their function as signal balancing complimentary circuit pathways, providing balanced, full-differential functionality.

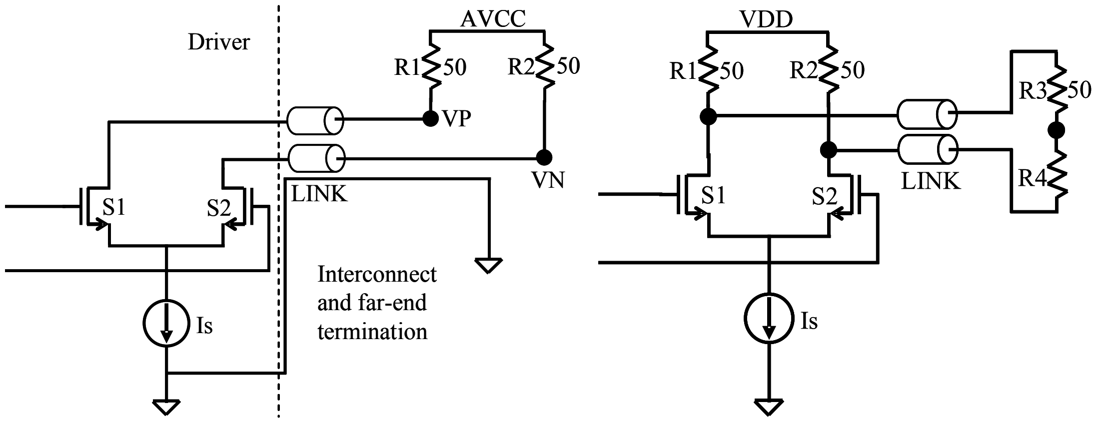

Figure 7: a) DVI driver schematic and b) simple LVDS driver schematic

Figure 7 illustrates two forms of electrical signal drive on differential interconnect. The schematic on the left shows a DVI driver schematic in accordance with **DVI 1.0**, and the one on the right is a simple **LVDS** driver. Whereas both drivers are designed and specified to create reduced voltage swings, a key difference between the two is in the nature of differential signal launch.

The **DVI** driver functions by alternately activating switch S1 and S2 corresponding to the symbol transmitted. This is not a fully differential driver, since one of the switches disconnects and 'floats' the transmit or source end of one wire of the pair while the other switch pulls a current through the complimentary wire. Since the current loop must be completed, the shield pathway, connecting to ground in the figure, serves as a return path, and is therefore explicitly included in the illustration for the line driver in the **DVI 1.0** specification [10]. This signaling architecture is therefore not truly or fully differential. The **LVDS** driver addresses this issue effectively through source-termination resistors R1 and R2 in the figure on the right. When switch S2 turns ON, and S1 simultaneously turns OFF, a current flows through R1 into one wire of the differential pair, and through far-end termination resistors R3, R4 back through the complimentary wire, and then through S2. With the termination resistors R3 and R4 'floated' at the far end of the link, the current flowing through one wire of the link is exactly equal in magnitude and opposite in direction to the current flowing through the complimentary wire of the link. **LVDS** therefore accomplishes fully-differential, or true-differential signaling. The presence of source and sink termination renders this signaling architecture very robust with respect to reflections from impedance discontinuities that may exist within the link; source termination also helps with minimizing the impact of cross-talk from adjacent signal wire pairs (NEXT) at the source end. This driver architecture is therefore much better suited for very high data rates and correspondingly necessary SI.

HDMI 1.3a [12] more than doubles the **DVI** data rate to 3.4Gbps per twisted wire pair, and therefore explicitly recommends source-termination through "*It is recommended that Sources capable of higher speeds incorporate an effective amount of source termination, especially if using Type C connectors*", thereby transforming pseudo-differential signaling in **DVI** to fully differential signaling in **HDMI**.

AC-coupling

Another well-known and advantageous technique that improves SI in long interconnects is AC–coupling, very commonly used in **LVDS** signaling. Systems interconnected by long cables have 'system ground' levels not at the same relative potential level with respect to a solid 'earth' connection for the facility. Such system ground differentials can introduce common-mode DC level shifts or other common-mode noise, despite the addition of a low-resistance shield path to the cable, into the differential signals within the cable that may degrade signaling performance and the link BER.

This problem is very effectively eliminated by the use of AC-coupling, where series capacitors connect the cable far-end points to termination impedances. Fully differential **LVDS** is particularly well-suited to this type of connection. AC-coupling provides not only the advantage of DC common-mode noise rejection, it also provides a level of signal high-pass filtering that de-emphasizes the lower frequency components and provides a measure of equalization. Additionally, it also eliminates the need for robust external shielding of cables containing fully differential signal pairs which are inherently immune to external radiation.

HDMI is therefore moving to this signaling architecture as may well be predicted. A recent article in the EETimes® print edition quotes HDMI Licensing LLC as saying that AC-coupling is the next enhancement for signaling on their agenda. The transformation of **DVI** signaling to **fully differential in HDMI** through source termination facilitates this shift. It is interesting that HDMI is gradually incorporating all of the best practices of LVDS in order to accomplish high data rates and/or long reach.

Symmetric Class-B Differential Signaling

An aspect of signaling discussed early in this paper is **signal gain**, which becomes necessary in long cables at high data rates because of the attenuation in the cable transfer function. Reference [9] that deals with remote video distribution on Cat-5 cables indicates that "*Putting all of the gain on the drive side maximizes the signal-to-noise ratio*". This is made possible in binary signaling through the use of ComLSI's **Class-B Differential Signaling** (**CBDS**) technology.

LVDS, DVI and HDMI are all encumbered by the legacy constraint of low-voltage-swing signaling, which while being quite helpful from a power, performance and EMI standpoint, can also be a limitation in signaling through long cables. LVDS for example is defined as a maximum voltage swing of 454mV as per the EIA standard, and DVI and HDMI indicate voltage swings that are nominally around approximately 600mV. With attenuating factors as high as 30dB, not considering termination losses (6dB or a factor of ½), a swing of even 600mV will be attenuated down to approximately 20mV, which could lead to greatly reduced SNR despite corrective measures for ISI, NEXT and FEXT (near-end and far-end cross-talk). Gain at the receiver end does not help as much here, since dominant components of noise in the signal are spectral components of the same frequency as that of the signal.

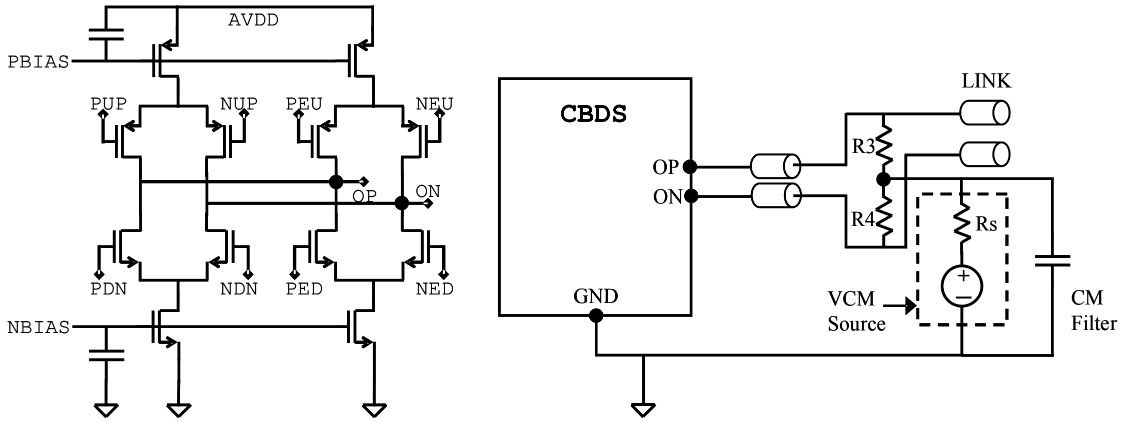

Figure 8: a) CBDS Line Driver output stage, b) CBDS or LVDS external termination

It is important, therefore, that the signal be amplified at the drive end and then transmitted. This is accomplished by the **CBDS** driver that is capable of as much as 14mA (4X of LVDS or higher) of total current flow into and out of the true and complement wires. This is accomplished without any additional static current consumption by the Class-B or Push-Pull architecture as illustrated in figure 8. Into 100Ohm termination impedance, therefore, **CBDS** drivers are capable of as much as **1.4V swing**. Class-B drive also provides symmetrical drive architecture, with well-matched, identical current sources driving currents into and out of the wires, as opposed to some LVDS implementations that connect a current source to one wire and a terminating impedance from the opposite voltage reference to another wire. The symmetrical drive coupled with very closely matched push and pull currents as well as minimized intra-pair skew helps eliminate electro-magnetic radiation from unshielded signal pairs despite the high voltage swings in **CBDS**.

While source (transmitter) termination is not essential for **CBDS** drivers, the improvement in SI with source termination assists in enhancing data rates through long cables. An example of source termination is illustrated in figure 8; DC as well as AC termination assists in minimizing the impact of noise or intra-pair skew. Class-B output stages are susceptible to differential power supply noise that may be coupled into the signal pair. Additionally, they are also susceptible to common-mode voltage differences between the true and complement wires. These issues are addressed effectively through careful bias circuit design, decoupling as well as common-mode termination.

Summary

A number of aspects impacting SI and techniques enhancing the quality of high-speed signal transmission through long cables have been discussed. The development of **DVI** electrical recommendations into **HDMI 1.3** released recently shows a clear trend toward the adoption of best known practices from **LVDS** related industry developments. Examples include source-termination that renders HDMI signals fully differential, and the reported inclusion of AC-coupling in future releases of HDMI that mirrors best practices in long links based upon the LVDS standard. Sink equalization in HDMI further rationalizes the link architecture.

We also introduce symmetric, class-B, true-differential signaling (**CBDS**) technology capable of 4 times or greater voltage swings as compared with LVDS while retaining all of its benefits, enabling very long cable based interconnect links.

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